Amendments to the Specification:

a. Please replace Paragraph **[0011]** with the following amended paragraph:

[0011] Conventional nonvolatile memory requires three terminal MOSFET-based devices. The layout of such devices is not ideal, usually requiring an area of at least $8f^2$ for each memory cell, where f is the minimum feature size. However, not all memory elements require three terminals. If, for example, a memory element is capable of changing its electrical properties (e.g., resistivity) in response to a voltage pulse, only two terminals are required. With only two terminals, a cross point array layout that allows a single cell to be fabricated to a size of $4f^2$ can be utilized. Co-pending U.S. patent application, "Cross Point Memory Array Using Multiple Thin Films," U.S. Application No. 10/330,512, filed December 26, 2002, **now issued U.S. Patent 6,753, 561,** incorporated herein by reference in its entirety and for all purposes, describes such a device.

b. Please replace Paragraph **[0015]** with the following amended paragraph:

[0015] FIG. 1B depicts an exemplary stacked cross point array 150 employing four memory layers 155, 160, 165, and 170. The memory layers are sandwiched between alternating layers of x-direction conductive array lines 175, 180 and 185 and y-direction conductive array lines 190 and 195 such that each memory layer 155, 160, 165, and 170 is associated with only one x-direction conductive array line layer and one y-direction conductive array line layer. Although the top conductive array line layer 185 and bottom conductive array line layer 175 are only used to supply voltage to a single memory layer 155 and 170, the other conductive array line layers 180, 190, and 195 can be used to supply voltage to both a top and a bottom memory layer 155, 160, 165, or 170. Co-pending U.S. patent application, "Re-Writable Memory With Multiple Memory Layers," U.S. Application No. 10/612,191, filed July 1, 2003, **now issued U.S. Patent 6,906,939,** incorporated herein by reference in its entirety for all purposes, describes stacked cross point arrays.

c. Please replace Paragraph **[0017]** with the following amended paragraph:

[0017] One benefit of the cross point array is that the active circuitry that drives the cross point array 100 or 150 can be placed beneath the cross point array, therefore reducing the footprint required on a semiconductor substrate. Co-pending U.S. patent application, "Layout Of Driver Sets In A Cross Point Memory Array," U.S. Application No. 10/612,733, filed July 1, 2003, incorporated herein by reference in its entirety for all purposes, describes various circuitry that can achieve a small footprint underneath both a single layer cross point array 100 and a stacked cross point array 150. Further details of the peripheral circuitry are described in co-pending U.S. patent application, "An Adaptive Programming Technique for a Re-Writeable Conductive Memory Device," U.S. Application No. 10/680,508, filed October 6, 2003, **now issued U.S. Patent 6,940,744,** incorporated herein by reference in its entirety for all purposes. **FIG. 6A depicts x-direction driver sets 605, 610, and 615 that are used to select specific x-direction conductive array lines in a X_0 layer 175, X_1 layer 180, and X_2 layer 185. Although the X_0 driver 605 and the X_2 driver 615 can use identical logic, separate drivers are shown because of the difficulty in routing the single X_0 driver 605 around a thru 650 that connects the X_1 layer 180 to the X_1 driver 610. FIG. 6B depicts y-direction driver sets 620 and 625 that are used to select specific y-direction conductive array lines in the y-direction conductive array line layers 190 and 195. The Y_0 driver set 620 uses a thru 630 that goes through one ILD layer in order to connect with the Y_0 layer 190. The Y_1 driver set 625 uses a thru 635 that goes through three ILD layers in order to connect with the Y_1 layer 195.**

d. Please replace Paragraph **[0019]** with the following amended paragraph:

[0019] FIG. 3 is a generalized diagrammatic representation of a memory cell 300 that can be used in a transistor memory array. Each memory cell 300 includes a transistor 305 and a memory plug 310. The transistor 305 is used to permit current from the data line 315 to access the memory plug 310 when an appropriate voltage is applied to the select line 320, which is also the transistor's gate. The reference line 325 might span two cells if the adjacent cells are laid out as the mirror images of each other. Co-pending U.S. patent application, "Non-Volatile Memory with a Single Transistor and Resistive Memory Element," U.S. Application No. 10/249,848, filed May 12, 2003, **now issued U.S. Patent 6,856,536,** incorporated herein by reference in its entirety for all purposes, describes the specific details of designing and fabricating a transistor memory array.

e. Please replace Paragraph **[0020]** with the following amended paragraph:

[0020] Each memory plug 255 or 310 contains a multi-resistive state element (described later) along with any other materials that may be desirable for fabrication or functionality. For example, the additional materials might include a non-ohmic device, as is described in co-pending application "High Density NVRAM," U.S. Application No. 10/360,005, filed February 7, 2003, **now issued U.S. Patent 6,917,539,** incorporated herein by reference in its entirety for all purposes. The non-ohmic device exhibits a very high resistance regime for a certain range of voltages (V_{NO-} to V_{NO+}) and a very low resistance regime for voltages above and below that range. The non-ohmic device, either alone or in combination with other elements, may cause the memory plug 255 or 310 to exhibit a non-linear resistive characteristic. Exemplary non-ohmic devices include three-film metal-insulator-metal (MIM) structures and back-to-back diodes in series.

f. Please replace Paragraph **[0021]** with the following amended paragraph:

[0021] Furthermore, as described in "Rewriteable Memory With Non-Linear Memory Element," U.S. Application No. 10/604,556, filed July 30, 2003, **now issued U.S. Patent 6,870,755,** incorporated herein by reference in its entirety for all purposes, it may also be possible for the memory cell exhibit non-linear characteristics without a separate non-ohmic device. It should be noted that since it is possible for a memory cell to exhibit non-linear characteristics the terms "resistive memory" and "resistive device" also apply to memories and devices showing non-linear characteristics, and can also be referred to as "conductive memory" and "conductive device." While a non-ohmic device might be desirable in certain arrays, it may not be helpful in other arrays. Regardless, if certain treatments are used to improve the switching characteristics of the memory plug the treatments may also create an integrated non-ohmic device. Such a non-ohmic device may, therefore, be used even if it is not necessary in that type of array.

g. Please replace Paragraph **[0036]** with the following amended paragraph:

[0036] It should also be appreciated that fabrication of the multi-resistive state element might include additional techniques in order to ensure an effective memory device. For example, biasing the multi-resistive state element might be beneficial in order to ensure the hysteresis is presented in a certain direction. Co-pending U.S. patent application, "Multi-Layer Conductive Memory Device," U.S. Application No. 10/605,757, filed October 23, 2003, **now issued U.S. Patent 6,965,137,** incorporated herein by reference in its entirety for all purposes describes using a multi-layered multi-resistive state element in order to encourage a hysteresis in a certain direction. As previously discussed, a reactive metal can also be a desirable addition to the multi-resistive state element.

h. Please amend the section titled "**BRIEF DESCRIPTION OF THE DRAWINGS**" beginning on **page 5 of 25** of the **Specification** as follows:

BRIEF DESCRIPTION OF THE DRAWINGS

The invention may best be understood by reference to the following description taken in conjunction with the accompanying drawings, in which:

FIG. 1A depicts a perspective view of an exemplary cross point memory array employing a single layer of memory;

FIG. 1B depicts a perspective view of an exemplary stacked cross point memory array employing four layer of memory;

FIG. 2A depicts a plan view of selection of a memory cell in the cross point array depicted in FIG. 1A;

FIG. 2B depicts a perspective view of the boundaries of the selected memory cell depicted in FIG. 2A;

FIG. 3 depicts a generalized representation of a memory cell that can be used in a transistor memory array;

FIG. 4 depicts an exemplary flow chart of various processing steps that could be involved in fabrication of a memory;

FIG. 5A is a chart of measurements across a multi-resistive state memory element after a layer of reactive metal has been deposited; ~~and~~

FIG. 5B is a chart depicting the double ramp voltage pulse used to for the measurements of FIG. 5A [[.]] ;

FIG. 6A depicts a schematic diagram of x-direction driver sets; and

FIG. 6B depicts a schematic diagram of y-direction driver sets.

It is to be understood that, in the drawings, like reference numerals designate like structural elements. Also, it is understood that the depictions in the ~~FIGs.~~ FIGS. are not necessarily to scale.